

Please cancel claims 44 and 46.

Please amend the claims as follows:

Sub D1
28. (Amended) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

C1
the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers in only the n-channel TFT,

the active layer includes a low concentration impurity region that is in contact with a channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

30. (Amended) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, characterized in that:

C2
the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers in only the n-channel TFT; and

the second wiring line has a portion of structure laminated with a first conductive layer and a second conductive layer, and a portion of structure wrapped a third conductive layer with the first conductive layer and the second conductive layer.

31. (Amended) A semiconductor device according to claim 30, characterized in that the third conductive layer has a lower resistance value than the first conductive layer or the second conductive layer.

C3
33. (Amended) A semiconductor device according to claim 30, characterized in that the third conductive layer is appropriately a conductive film mainly containing aluminum (Al) or copper (Cu).

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34. (Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed in n-channel TFT, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers,

the active layer includes a low concentration impurity region that is in contact with a channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

C3

35. (Amended) A semiconductor device according to claim 34, characterized in that the first wiring line is kept at a ground electric potential or at a source power supply electric potential.

36. (Amended) A semiconductor device according to claim 34, characterized in that the first wiring line is kept at a floating electric potential.

37. (Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed in an n-channel TFT, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers,

the second wiring line has a portion of structure laminated with a first conductive layer and a second conductive layer, and a portion of structure wrapped a third conductive layer with the first conductive layer and the second conductive layer.

38. (Amended) A semiconductor device according to claim 37, characterized in that the third conductive layer has a lower resistance value than the first conductive layer or the

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second conductive layer.

04 40. (Amended) A semiconductor device according to claim 37, characterized in that the third conductive layer is appropriately a conductive film mainly containing aluminum (Al) or copper (Cu).

41. (Amended) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on a same substrate, characterized in that:

a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit have a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers; and

the first wiring line connected to the pixel TFT is kept at a fixed electric potential or a floating electric potential, and the first wiring line connected to the n-channel TFT included in the driver circuit is kept at a same level of electric potential as the second wiring line connected to the n-channel TFT included in the driver circuit.

42. (Amended) A semiconductor device according to claim 41, characterized in that the active layer includes a low concentration impurity region that is in contact with a channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

C5 47. (Amended) A semiconductor device according to any one of claims 28 to 46, the semiconductor device is an active matrix liquid crystal display or an active matrix EL display.

48. (Amended) A semiconductor device according to any one of claims 28 to 46, the semiconductor device is selected from a video camera, a digital camera, a projector, a

C5 projection TV, a goggle type display, an automobile navigation system, a personal computer,
or a portable information terminal.
